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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,019	11/28/2001	John Whitman	4294.2US (98-1208.2)	6139

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

K.D

Office Action Summary	Application N .	Applicant(s)	
	09/997,019	WHITMAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- Th MAILING DATE of this communication appears on the c ver sheet with th c rresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 6, 7, and 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (US/6,461,932).

The rejection that set forth in the Office action that was mailed on August 29, 2003 is maintained and repeated herein below as record.

Re claim 1, Wang discloses a method for preparing a surface of a semiconductor device structure for planarization, comprising: providing a semiconductor device structure (see Fig. 4d) including at least one recess (54) (i.e., trench in the silicon substrate (40)) formed in a surface thereof and a first material layer (56) substantially filling the at least one recess (54) and covering the surface (not labeled), the first material layer (56) having a non-planar surface (see Fig. 4d); applying a second material (60) to the first material layer (56); and spreading the second material (60) over the first material layer (56) so as to forming a second material layer (60) having a substantially planar surface (see Col. 6, lines 29-37) without requiring subsequent planarization of the second material (see Fig. 4d).

Re claim 2, as applied to claim 1 above, Wang discloses all the claimed limitations including the limitation wherein the applying said second material comprises applying a stress buffer material to the first material layer (see Fig. 4d).

Re claim 6, as applied to claim 1 above, Wang discloses all the claimed limitations including the limitation wherein said providing comprises providing a shallow trench isolation structure with the at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure (see Fig. 4d).

Re claim 7, as applied to claim 6 above, Wang discloses all the claimed limitations including the limitation providing the shallow trench isolation structure with the first material layer comprising an electrical insulator material (see Figs. 4d-4g).

Re claim 10, as applied to claim 2 above, Wang discloses all the claimed limitations including the limitation wherein the spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of said first material layer substantially uncovered by the stress buffer material (see Figs. 4d and 4e).

Re claim 11, as applied to claim 10 above, Wang discloses all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 4d and 4e).

Re claim 12, as applied to claim 11 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material (see Figs. 4d and 4e).

Re claim 13, as applied to claim 12 above, Wang discloses all the claimed limitations including the limitation wherein said etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material (see Figs. 4d and 4e).

Re claim 14, as applied to claim 13 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing further comprises abrasively planarizing the stress buffer material and the at least one region to expose the surface of said semiconductor device structure adjacent the at least one recess, said surface of the semiconductor device structure and a surface of thefirst material layer in the at least one recess being located in substantially the same plane following said planarizing (see Figs. 4d and 4e).

Re claim 15, as applied to claim 13 above, Wang discloses all the claimed limitations including the limitation wherein said plananizing further comprises concurrently etching said first material layer and the stress buffer material at substantially the same rate so as to expose said surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of said first material layer in the at least one recess being located in substantially the same plane following said plananizing (see Figs. 4d-4f).

Re claim 16, as applied to claim 11 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing is effected until said surface of said semiconductor device structure is exposed through the first material layer (see Figs. 4d-4e).

Re claim 17, as applied to claim 16 above, Wang discloses all the claimed limitations including the limitation wherein the etching is effected until a surface of the first material layer

in the at least one recess is in substantially the same plane as the surface of said semiconductor device structure (see Figs. 4d-4f).

Re claim 18, as applied to claim 16 above, Wang discloses all the claimed limitations including the limitation removing the stress buffer material from the semiconductor device structure (see Figs. 4d-4f).

Re claim 19, as applied to claim 2 above, Wang discloses all the claimed limitations including the limitation wherein the spreading comprises forming a substantially planar surface over the semiconductor device structure (see Figs. 4d-4f).

Re claim 20, as applied to claim 19 above, Wang discloses all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 4d-4f).

Re claim 21, as applied to claim 20 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises substantially concurrently abrasively planarizing the stress buffer material and the first material layer to surface of said semiconductor device expose the device structure adjacent the at last one recess, said surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following the planarizing (see Figs. 4d-4f).

Re claim 22, as applied to claim 20 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises substantially concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of said semiconductor device structure adjacent the at least one recess with said surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following said planarizing.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Wang (US/6,461,932) in view of Yoshihara (US/6,117,486).

The rejection that set forth in the Office action that was mailed on August 29, 2003 is maintained and repeated herein below as record.

Re claims 3-5, as applied to claim 1 above, Wang discloses all the claimed limitations. Although is a well-known process, Wang does not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while

allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Wang reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Wang (US/6,461,932) in view of Hsich (US/6,228,711).

The rejection that set forth in the Office action that was mailed on August 29, 2003 is maintained and repeated herein below as record.

Re claims 8 and 9, as applied to claim 1 above, Wang discloses all the claimed limitations. Although it is well-known in the art, Wang does not specifically disclose providing dual-damascene structure.

Hsich discloses forming of dual-damascene structure and forming a conductive layer over the dual-damascene structure (see Fig. 3H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Wang reference with dual-damascene

structure as taught by Hsich. because, as well-known in the art, the structure would have increased the device density.

Response to Arguments

6. Applicants' arguments filed December 1, 2003 have been fully considered but they are not persuasive.

With respect to claims rejection (i.e., claims 1, 2, 6, 7, and 10-22) under 35 U.S.C. § 102, Applicants argued that "Wang lacks any express or inherent description of spreading second material layer over a first material layer so as to form a second material layer having a substantially planar surface, as recited in independent claim 1. Instead, Wang describes a smoothening layer 60 that may include slight depressions" in the upper smoothening surface 62 thereof . . . "

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that Wang '932 discloses all the claimed limitation as applied on Paragraph 2 herein above.

In response to applicants' argument that Wang lacks any express or inherent description that "spreading second material layer over a first material layer so as to form a second material layer having a substantially planar surface," the Examiner respectfully submits applicants assertion lack validity because applicants' own taking (interpretation) of the Wang '932 reference, as stated in Page 6 of applicants remark, refutes the applicants' assertion because applicants admittedly stated that "Wang describes a process for creating a trench-isolated semiconductor structure using a pre-smoothing technique to avoid difficulties such as dishing

and premature silicon-nitride removal that might otherwise occur during chemical-mechanical polishing. .." (hereinafter CMP"). Col. 4, ln. 48 - 51. The process includes providing a dielectric layer over a

semiconductor surface, which is covered with a smoothening layer" whose upper surface is smoother than the upper surface of the dielectric layer. Col. 6, ln. 29-31. The smoothening layer is applied either by a **deposition/spinning** procedure" (Co1. 6, ln. 52 - Col.7, ln. 14), deposition/flow" procedure (Co1. 7, ln. 15-27), or a combination of these procedures (Col. 7, ln. 28-41)." As clearly shown in Fig. 4d, the surface smoothening layer 60 (i.e., second material) is deposited and spread over the first material layer (56) and this process also clearly admitted by the applicants in their remarks as set forth herein above.

In response to applicants argument that "Wang describes a smoothening layer 60 that may include slight depressions" in the upper smoothening surface 62 thereof," the Examiner respectfully submits that Wang discussion is that the probability that "may" exist a slight depression which can be true for the instant application depression layer. As shown in Fig. 4D Wang '932 discloses a planar layer and no where in Wang '932 reference is disclosed that the smoothening layer 62 is not planar and the rejected claims also do not provide degree of planarity or smoothness of the planar surface. Furthermore, the rejected claim, in particular claim 1, recites "spreading the second material over the first material layer so as to forming a second material layer having a **substantially planar surface.**" The broad interpretation of "**substantially planar surface**" is "being largely planar" but not "absolutely planar" which is consistent with Wang's disclosure. Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44

USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the rejection of claims 1, 2, 6, 7, and 10-22 under 35 U.S.C. § 102 is deemed proper.

With respect to claims rejection (i.e., 3-5) under 35 U.S.C. § 103, Applicants argued that "one of ordinary skill in the art would not have been motivated to combine the teachings of Wang with those of Yoshihara to provide a method of providing a substantially planar upper surface of a material applied over the top of a substrate having a non-planar upper surface, such as a dielectric material. Such a configuration of layers necessarily requires the overlying material to have a non-uniform thickness . . . "

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that the combination Wang '932 and Yoshihara '486 disclose all the claimed limitation as applied on Paragraph 4 herein above.

The difference between the Wang '932 and the instant application is that, although Wang teaches spin coating of resist layer, Wang does not specifically teach applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm. Wang teaches spin coating but the issue is why one ordinary skill in the art use different

revolution (rpm) (i.e., optimize process) during the spin coating process of the resist layer. Therefore, such teaching is disclosed in Yoshihara et al. '486 teachings. Hence, one of ordinary skill in the art would have motivated to combine the teachings of Wang '932 and Yoshihara to come up with the instant application claimed invention at the time of the invention is made. It is obviously clear that one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Therefore, the *prima facie* case of obviousness has been met and the rejection of claims 3-5 under 35 U.S.C. § 103 is deemed proper.

With respect to claims rejection (i.e., claim 8 and 9) under 35 U.S.C. § 103, applicants argument is solely based since claim 1 is allowable and claims 8 and 9 are also allowable. In response to the applicants' argument, the Examiner respectfully submits that such an argument is

not commensurate with the scope of the claims, in particularly, as stated above. In addition, the Examiner respectfully submits that claim 1 is not allowable because it lacks novelty and claim 8 and 9 are also not allowable because the claims do not present novel and non-obvious subject matter as applied in Paragraph 5 herein above.

Therefore, the *prima facie* case of obviousness has been met and the rejection of claims 8 and 9 under 35 U.S.C. § 103 is deemed proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
February 11, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER